REMARKS

In response to the pending Office Action, Applicants have amended the specification so as to address the issues raised in the Office Action. It is believed that each of the formal matters, except those noted below, identified by the Examiner on pages 2-3 of the Office Action have been corrected by the foregoing amendments. Applicants wish to thank the Examiner for his assistance improving the clarity of the specification.

It is noted that the use of the term "damascene" was questioned. However, "damascene processes" are well known to those of skill in the art. Applicants have attached Abstracts of three US patents which utilize the term in question. Accordingly, as it is preferably to omit from specifications discussions regarding subject matter which is well known in the art, it is respectfully submitted there is no reason to amend the specification to contain a further description of damascene processes.

In addition, it was requested that page 17, line 25 and page 20, line 2 be amended to further clarify the reference to the "drawings". However, upon review of the specification, it is clear that the "drawings" referred to in these portions of the specification are identified in the subsequent paragraphs, and this fact is indicated in the specification. Accordingly, it is respectfully submitted that the current language is neither misleading nor inaccurate, and therefore, there is no need to make any further amendments thereto.

Serial No.: 09/988,017

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

Respectfully submitted,

McDERMOTT, WILL & EMERY

Date: 2/17/04

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United States Patent **6,689,681**
Watanabe **February 10, 2004**

Semiconductor device and a method of manufacturing the same

Abstract

A semiconductor device includes a first insulating layer which is formed above a semiconductor substrate including a plurality of semiconductor elements and which includes lower-layer damascene wiring, a second insulating layer which is formed on the first insulating layer and which includes a second damascene wiring and an aligning wiring pattern forming a first step, and a first aligning surface wiring pattern including a surface wiring pattern to cover the second damascene wiring and a first aligning surface wiring pattern which is formed on the aligning wiring pattern and which has a second step reflecting the first step. The surface wiring pattern and the first aligning surface wiring pattern are formed using one surface wiring layer. A novel multilayer wiring structure thus obtained is suitably manufactured by the ***damascene process***.

Inventors: **Watanabe; Kenichi** (Kawasaki, JP)
Assignee: **Fujitsu Limited** (Kawasaki, JP)

Appl. No.: **242623**
Filed: **September 13, 2002**

Foreign Application Priority Data

Apr 13, 2001[JP] 2001-115501

Current U.S. Class: **438/633**; 438/638; 438/975; 257/E21.577; 257/E21.579
Intern'l Class: H01L 021/476.3
Field of Search: 438/587,622-633,637-638,618,975,FOR 435
257/E21.577,E21.579,E23.152

References Cited [Referenced By]

U.S. Patent Documents

6333519 Dec., 2001 Nakazawa.

United States Patent **6,680,252**
Chen , et al. **January 20, 2004**

Method for planarizing barc layer in dual damascene process

Abstract

The present invention is directed to a method for planarizing BARC layer in dual ***damascene process***. For forming a dual damascene interconnect structure, by use of the present invention, a planar topography of the BARC layer is achieved by chemical mechanical polishing. The present invention applies a low temperature to bake the coated BARC layer before BARC material cross-links and induces the anti-reflective characteristic. Then, the BARC layer is planarized by chemical mechanical polishing. Next, a high temperature baking of the BARC layer is provided before coating the photoresist, so formation of the BARC layer is controlled with minimized variation in surface level and has the antireflective characteristic. Thus, the profile distortion on the via and the critical dimension control for the via are improved by patterning the via on a planar and an anti-reflective surface.

Inventors: **Chen; Anseime** (Hsin-Chu, TW); **Huang; Hui-Ling** (Hsin-Chu, TW); **Chang; Vencent** (Taipei, TW); **Chang; Andersen** (Miao-Li, TW)
Assignee: **United Microelectronics Corp.** (Hsin-Chu, TW)
Appl. No.: **854966**
Filed: **May 15, 2001**

Current U.S. Class: 438/691; 438/692
Intern'l Class: H01L 021/302
Field of Search: 438/700,690-693,720,723,724,725

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U.S. Patent Documents

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United States Patent **6,686,643**
Schwarzl , et al. **February 3, 2004**

Substrate with at least two metal structures deposited thereon, and method for fabricating the same

Abstract

Metal structures that can be produced by a ***damascene process*** are disposed in a first insulating layer and a second insulating layer is disposed above the latter. There is in each case at least one cavity which is disposed between the metal structures, is disposed in the first insulating layer and is covered by the second insulating layer. The cavities and the metal structures are produced next to one another by self-aligned process steps.

Inventors: **Schwarzl; Siegfried** (Neubiberg, DE); **Pamler; Werner** (Munchen, DE); **Gabric; Zvonimir** (Zorneding, DE)
Assignee: **Infineon Technologies AG** (Munich, DE)

Appl. No.: **725346**
Filed: **November 29, 2000**

Foreign Application Priority Data

Nov 29, 1999[DE] 199 57 302

Current U.S. Class: **257/522**; 257/758
Intern'l Class: H01L 029/00
Field of Search: 257/760,752,753,758,762,763,522

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U.S. Patent Documents

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5949143	Sep., 1999	Bang	257/758.
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